

INFORMATION DISCLOSURE CITATION IN AN APPLICATION		ATTY. DOCKET NO. 50006-188		SERIAL NO. 10/787240	
		APPLICANT Hans Jurgen MATTAUSCH, et al.			
(PTO-1449)		FILING DATE February 27, 2004		GROUP 2189	
U.S. PATENT DOCUMENTS					
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ₂ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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KV		H.J. MATTAUSCH, "Hierarchical architecture for area-efficient integrated N-port memories with latency-free multi-gigabit per second access bandwidth", Electronics Letters, 19th August 1999, Vol. 35, No. 17, pages 1-2.			
KV		N. OMORI et al., "Compact central arbiters for memories with multiple read/write ports", Electronics Letters, 21st June 2001, Vol. 37, No. 13, pages 811-813 (w/ English Translation).			
KV		H.J. MATTAUSCH, "Area-Efficient Multi-Port SRAMs for On-Chip Data-Storage with High Random-Access Bandwidth and Large Storage Capacity", IEICE Trans. Electron., Vol. E84-C, No. 3, March 2001, pages 410-418.			
EXAMINER <i>Kevin Verheij</i>		DATE CONSIDERED <i>5/26/06</i>			

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